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cont'd  
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24. (New) The voltage source according to claim 14, wherein the ferrite bead and the capacitor form a resistor divider circuit to assist in noise signal removal.

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**REMARKS**

This paper is responsive to the paper indicated above, and is responsive in any other manner indicated below.

**PENDING CLAIMS**

Claims 1-16 were pending, under consideration and subjected to examination in the Office Action. Unrelated to any prior art rejection, appropriate claims have been amended and/or added in order to adjust a clarity and/or focus of Applicant's claimed invention. At entry of this paper, Claims 1-24 will be pending for further consideration and examination in the application.

**ALL REJECTIONS UNDER 35 USC §§102 AND 103 - TRAVERSED**

All 35 USC rejections (i.e., the 35 USC §102 rejection of claims 1 and 9 as being anticipated by Vince (U.S. Patent 5,068,631), and the 35 USC §103 rejection of claims 2-8 and 10-16 as being unpatentable over Vince) are respectfully traversed, but such rejections have been rendered moot by the present clarifying amendments to Applicant's claims. Applicant respectfully submits the following in order to preclude renewal of such rejection with respect to Applicant's clarified and added claims.

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All descriptions of Applicant's disclosed and claimed invention, and all descriptions and rebuttal arguments regarding the applied prior art, as previously submitted by Applicant in any form, are repeated and incorporated hereat by reference. Further, all Office Action statements regarding the prior art rejections are respectfully traversed. As additional arguments, Applicant respectfully submits the following.

In order to properly support a §102 anticipatory-type rejection, any applied art reference must disclose each and every limitation of any rejected claim. The applied art does not adequately support a §102 anticipatory-type rejection because, at minimum, such applied art does not disclose (or suggest) the following discussed limitations of Applicant's claims.

Applicant's disclosed and claimed invention is directed toward providing arrangements to suppress noise with respect to inputs for a clock generator. In order to accomplish the same, Applicant's disclosed and claimed invention (e.g., independent claim 1, and claims dependent therefrom) advantageously utilizes a ferrite bead disposed along the voltage input line, with the ferrite bead having a first resistance. A bulk capacitor is also connected between an output side of the ferrite bead and ground (i.e., electrically between the ferrite bead and the clock generator), with the bulk capacitor having a substantially equivalent series resistance to the first resistance. The ferrite bead and the capacitor are provided in an "L" shaped filter configuration (see added claims 17, 19, 21, 23), and form a resistor divider circuit to assist in noise signal removal (see added claims 18, 20, 22, 24). Other ones of Applicant's other sets of independent claims and claims dependent therefrom have

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similar or analogous limitations to those of independent claim 1 and claims dependent therefrom.

Turning now to preclusion of the applied art, Vince is directed to electromagnetic filtering for a VLSI device having multiple power input leads. The Vince filtering arrangements make use of ferrite beads (FB) 109, as well as a plurality of capacitors (e.g., 108, 107-1, etc). It is respectfully noted that the capacitors 107-1, 107-2, 107-3 and 107-4 are decoupling capacitors (see, e.g., Vince's column 2, lines 24-25).

As a first difference between Vince and Applicant's clarified claims, it is noted that Applicant's bulk capacitor 20 (Applicant's FIG. 2) is disposed on an output side of the ferrite bead, whereas Vince's bulk capacitor 108 is disposed on an input side of Vince's ferrite bead. Still further, it is respectfully noted that, whereas Applicant's invention is provided in an "L" shaped filter configuration, Vince's arrangements are provided in a "π" shaped filter configuration (using Vince's bulk capacitor 108 and decoupling capacitor 107-1). Even further still, while Applicant's invention is disclosed and claimed as including a bulk capacitor having a substantially equivalent series resistance to the ferrite bead resistance (thus forming a resistor divider circuit to assist in noise signal removal), Vince's disclosure nowhere discusses any resistance values.

It is well known in the filter design art, that even a simple change in filter configuration and/or parameters of components within a configuration can very seriously affect a filter's response characteristics. Vince has three substantial differences from Applicant's disclosed and claimed invention, i.e., (1) the bulk capacitor is on a ferrite bead input side (as opposed to the output side), (2) un-

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discussed and therefore unknown ferrite-bead/capacitor resistance values, and, (3) a "π" shaped filter configuration (as opposed to an "L" shaped filter configuration). Accordingly, it is respectfully submitted that Vince's arrangements will operated drastically different from Applicant's disclosed and claimed filtering arrangements. Still further, it is respectfully submitted that it would not have been obvious to modify Vince's arrangement in a manner to arrive at Applicant's disclosed and claimed invention. More particularly, the Vince reference itself (i.e., without the hind sight knowledge of Applicant's invention) must provide the suggestion to modify. There are hundreds, if not thousands, of modifications which may be made to the Vince et al. arrangements. Vince, itself, nowhere discloses or suggest that modification "might result in increased filter performance or optimization" (as was argued within the Office Action remarks). Instead, it is respectfully submitted that the Office Action remarks concerning an "increased filter performance" or "optimization" incentive are gained only from the hindsight knowledge of Applicant's invention.

As a result of all of the foregoing, it is respectfully submitted that the previously applied art would not support a §102 anticipatory-type rejection or §103 obviousness-type rejection of Applicant's clarified claims. Accordingly, reconsideration and withdrawal of such §102 and §103 rejections, and express written allowance of all of Applicant's clarified and added claims, are respectfully requested.

#### **SPECIFIC TRAVERSAL OF "OFFICIAL NOTICE"**

Office Action comments in support of the art rejection(s) assert that certain claimed features were well known in the art, i.e., without providing supportive art

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references for such assertion. With regard to such assertion of apparent judicial (i.e., Examiner) notice of common knowledge or well-known prior art, attention is directed to MPEP §2144.03 which states, "If the applicant traverses such an assertion the examiner should cite a reference in support of his or her position." Accordingly, in view of Applicant's traversal in this regard, and in accordance with the provisions of MPEP §2144.03, Applicant respectfully requests that a documentary proof be cited to explicitly show that such features were explicitly known in the art, or alternatively, Applicant respectfully requests withdrawal of all rejections based upon such unsupported judicial notice. Further, at this point, it is respectfully submitted as a reminder that, if new art is now cited against any of Applicant's unamended claims, then it would not be proper to make a next action final.

#### **INDICATION OF CHANGES MADE**

In order to comply with requirements under the recent changes to U.S. practice, amendments are made via the attached "Appendix - Version With Markings To Show Changes Made".

#### **EXAMINER INVITED TO TELEPHONE**

The Examiner is herein invited to telephone the undersigned attorneys at the local Washington, D.C. area telephone number of 703/312-6600 for discussing any Examiner's Amendments or other suggested actions for accelerating prosecution and moving the present application to allowance.

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**CONCLUSION**

In view of the foregoing amendments and remarks, Applicant respectfully submits that the claims listed above as presently being under consideration in the application are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

To the extent necessary, applicant petitions for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to ATSK Deposit Account No. 01-2135 (as Order No. 219.39043X00), and please credit any overpayment of fees to such Deposit Account.

Respectfully submitted,



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ATTACHMENTS:  
Appendix-Version With Markings  
Form PTO-2038

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**APPENDIX - VERSION WITH MARKINGS TO SHOW CHANGES MADE****IN THE CLAIMS:**

Please amend the claims as follows. Note that the full text of all claims (including those not being amended within this paper) may also be included to provide the convenience of a complete set of claims for easy review:

1. (Amended) A circuit for removing noise on a voltage input line, comprising:  
a ferrite bead connected in [said] the voltage input line, the ferrite bead having a first resistance; and  
a bulk capacitor connected between an output side of [said] the ferrite bead and ground, the bulk capacitor having a substantially equivalent series resistance to the first resistance.
2. (Amended) The circuit according to claim 1, wherein [said] the capacitor is a D case tantalum bulk capacitor.
3. (Amended) The circuit according to claim 2, wherein [said] the capacitor has [a] the series resistance of approximately 0.8 Ohms.
4. (Amended) The circuit according to claim 1, wherein the ferrite bead has [a] the first resistance of approximately 0.3 Ohms.
5. (Amended) A voltage supply device comprising:

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a voltage source including a voltage regulator section producing a voltage output;

a ferrite bead connected at one side to [said] the voltage output and forming at another side an output, the ferrite bead having a first resistance; and

a capacitor connected between [said] the output and ground, the capacitor having a substantially equivalent series resistance to the first resistance;

where switching regulator noise from [said] the voltage regulator section [being removed] is removable by [said] the ferrite bead and capacitor.

6. (Amended) The voltage supply device according to claim 5, wherein [said] the capacitor is a D case tantalum bulk capacitor.

7. (Amended) The voltage supply device according to claim 5, wherein [said] the capacitor has [a] the series resistance of approximately 0.8 Ohms.

8. (Amended) The voltage supply device according to claim 5, wherein the ferrite bead has [a] the first resistance of approximately 0.3 Ohms.

9. (Amended) A method of removing switching regulator noise from a voltage supply line, comprising:

connecting a ferrite bead in [said] the voltage input line, the ferrite bead having a first resistance; and



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connecting a bulk capacitor between an output side of [said] the ferrite bead and ground, the capacitor having a substantially equivalent series resistance to the first resistance.

10. (Amended) The method according to claim 9, wherein [said] the capacitor is a D case tantalum bulk capacitor.

11. (Amended) The method according to claim 10, wherein [said] the capacitor has [a] the series resistance of approximately 0.8 Ohms.

12. (Amended) The method according to claim 9, wherein the ferrite bead has [a] the first resistance of approximately 0.3 Ohms.

13. (Amended) A voltage source for a clock circuit, comprising:  
a voltage regulator having [an] a regulator output;  
a ferrite bead connected to [said] the regulator output of [said] the voltage regulator and having an output, the ferrite bead having a first resistance; and  
a bulk capacitor connected to [said] the output of [said] the ferrite bead at one side and ground at another side, the bulk capacitor having a substantially equivalent series resistance to the first resistance;

wherein [said] the ferrite bead and capacitor act to remove switching regulator noise so as to produce an input voltage supply having a reduced switching regulator noise for [said] the clock circuit.

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14. (Amended) The voltage source according to claim 13, wherein [said] the capacitor is a D case tantalum bulk capacitor.

15. (Amended) The voltage source according to claim 14, wherein [said] the capacitor has [a] the series resistance of approximately 0.8 Ohms.

16. (Amended) The voltage source according to claim 13, wherein [said] the ferrite bead has [a] the first resistance of approximately 0.3 Ohms.

17. (New) The circuit according to claim 1, wherein the ferrite bead and the capacitor are provided in an "L" shaped filter configuration.

18. (New) The circuit according to claim 1, wherein the ferrite bead and the capacitor form a resistor divider circuit to assist in noise signal removal.

19. (New) The voltage supply device according to claim 5, wherein the ferrite bead and the capacitor are provided in an "L" shaped filter configuration.

20. (New) The voltage supply device according to claim 5, wherein the ferrite bead and the capacitor form a resistor divider circuit to assist in noise signal removal.

21. (New) The method according to claim 9, wherein the ferrite bead and the capacitor are provided in an "L" shaped filter configuration.

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22. (New) The method according to claim 9, wherein the ferrite bead and the capacitor form a resistor divider circuit to assist in noise signal removal.

23. (New) The voltage source according to claim 14, wherein the ferrite bead and the capacitor are provided in an "L" shaped filter configuration.

24. (New) The voltage source according to claim 14, wherein the ferrite bead and the capacitor form a resistor divider circuit to assist in noise signal removal.